

# SN5442A, SN54LS42, SN7442A, SN74LS42 4-LINE BCD TO 10-LINE DECIMAL DECODERS

SDLS109 – MARCH 1974 – REVISED MARCH 1988

- All Outputs Are High for Invalid Input Conditions
- Also for Application as  
4-Line-to-16-Line Decoders  
3-Line-to-8-Line Decoders
- Diode-Clamped Inputs

| TYPES | TYPICAL<br>POWER<br>DISSIPATION | TYPICAL<br>PROPAGATION<br>DELAYS |
|-------|---------------------------------|----------------------------------|
| '42A  | 140 mW                          | 17 ns                            |
| 'LS42 | 35 mW                           | 17 ns                            |

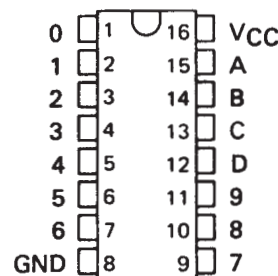
## description

These monolithic BCD-to-decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

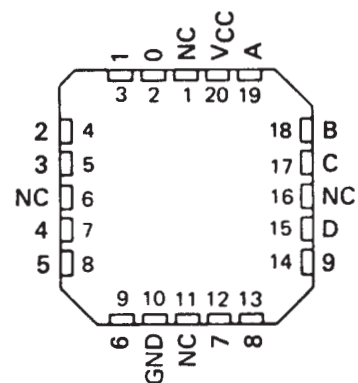
The '42A and 'LS42 feature inputs and outputs that are compatible for use with most TTL and other saturated low-level logic circuits. DC noise margins are typically one volt.

The SN5442A and SN54LS42 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN7442A and SN74LS42 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN5442A, SN54LS42 . . . J OR W PACKAGE  
SN7442A . . . N PACKAGE  
SN74LS42 . . . D OR N PACKAGE  
(TOP VIEW)



SN54LS42 . . . FK PACKAGE  
(TOP VIEW)

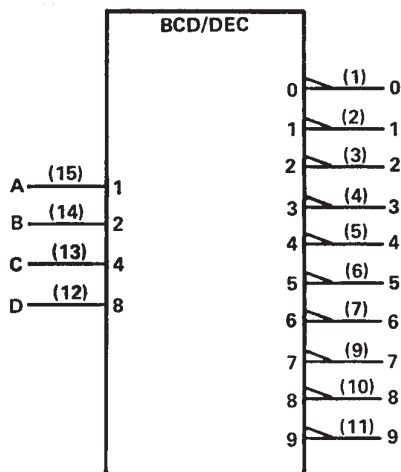


NC - No internal connection

# SN5442A, SN54LS42, SN7442A, SN74LS42 4-LINE BCD TO 10-LINE DECIMAL DECODERS

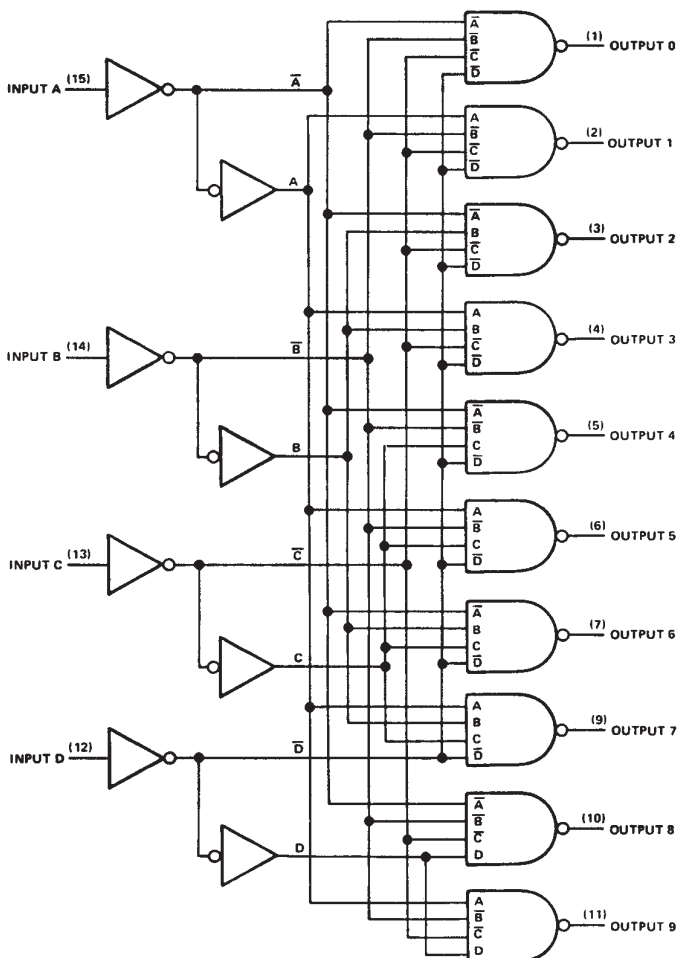
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

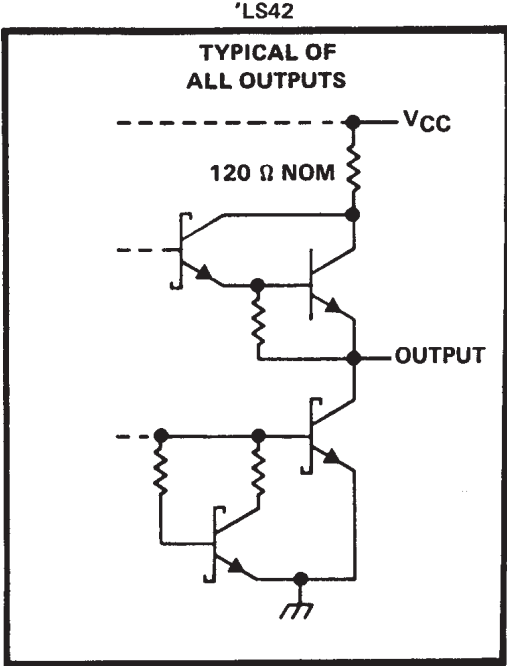
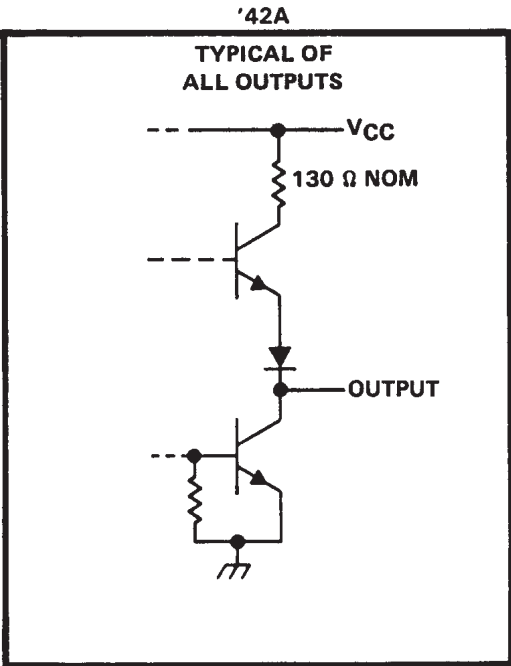
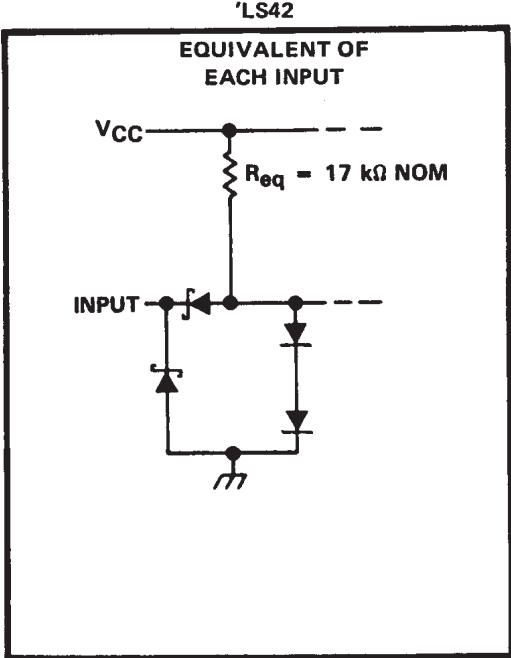
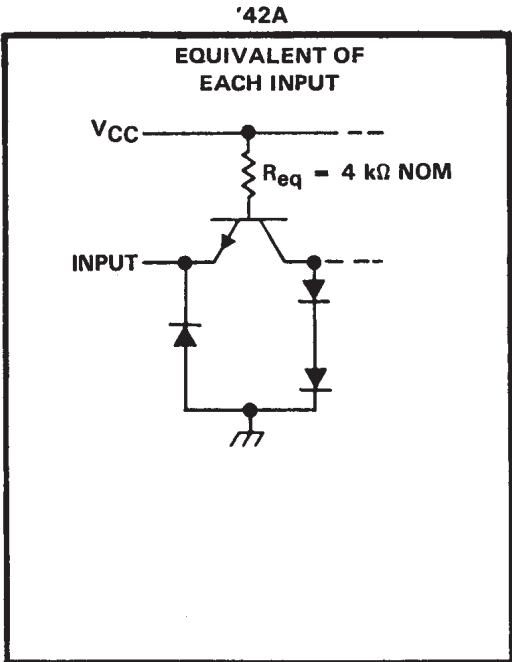


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SN5442A, SN54LS42, SN7442A, SN74LS42  
 4-LINE BCD TO 10-LINE DECIMAL DECODERS

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schematics of inputs and outputs





# SN5442A, SN54LS42, SN7442A, SN74LS42 4-LINE BCD TO 10-LINE DECIMAL DECODERS

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## recommended operating conditions

|                                       | SN5442A |     |      | SN7442A |     |      | UNIT         |
|---------------------------------------|---------|-----|------|---------|-----|------|--------------|
|                                       | MIN     | NOM | MAX  | MIN     | NOM | MAX  |              |
| Supply voltage, $V_{CC}$              | 4.5     | 5   | 5.5  | 4.75    | 5   | 5.25 | V            |
| High-level output current, $I_{OH}$   |         |     | -800 |         |     | -800 | $\mu$ A      |
| Low-level output current, $I_{OL}$    |         |     | 16   |         |     | 16   | mA           |
| Operating free-air temperature, $T_A$ | -55     |     | 125  | 0       |     | 70   | $^{\circ}$ C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER  | TEST CONDITIONS <sup>†</sup>   | SN5442A |                  |      | SN7442A |                  |      | UNIT    |
|--|--|---------|------------------|------|---------|------------------|------|---------|
|  |  | MIN     | TYP <sup>‡</sup> | MAX  | MIN     | TYP <sup>‡</sup> | MAX  |         |
| $V_{IH}$ High-level input voltage                  |  | 2       |                  |      | 2       |                  |      | V       |
| $V_{IL}$ Low-level input voltage                   |  |         |                  | 0.8  |         |                  | 0.8  | V       |
| $V_{IK}$ Input clamp voltage                       | $V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$  |         |                  | -1.5 |         |                  | -1.5 | V       |
| $V_{OH}$ High-level output voltage                 | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$ | 2.4     | 3.4              |      | 2.4     | 3.4              |      | V       |
| $V_{OL}$ Low-level output voltage                  | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$    |         | 0.2              | 0.4  |         | 0.2              | 0.4  | V       |
| $I_I$ Input current at maximum input voltage       | $V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$   |         |                  | 1    |         |                  | 1    | mA      |
| $I_{IH}$ High-level input current                  | $V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$   |         |                  | 40   |         |                  | 40   | $\mu$ A |
| $I_{IL}$ Low level input current                   | $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$   |         |                  | -1.6 |         |                  | -1.6 | mA      |
| $I_{OS}$ Short-circuit output current <sup>§</sup> | $V_{CC} = \text{MAX}$  | -20     |                  | -55  | -18     |                  | -55  | mA      |
| $I_{CC}$ Supply current                            | $V_{CC} = \text{MAX}, \text{ See Note 2}$  |         | 28               | 41   |         | 28               | 56   | mA      |

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

<sup>‡</sup> All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$ .

<sup>§</sup> Not more than one output should be shorted at a time.

NOTE 2:  $I_{CC}$  is measured with all outputs open and all inputs grounded.

## switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

| PARAMETER  | TEST CONDITIONS   | MIN | TYP | MAX | UNIT |
|--|---|-----|-----|-----|------|
| $t_{PHL}$ Propagation delay time, high-to-low-level output from A, B, C, or D through 2 levels of logic  | $C_L = 15 \text{ pF},$<br>$R_L = 400 \Omega,$<br>See Note 3 |     | 14  | 25  | ns   |
| $t_{PHL}$ Propagation delay time, high-to-low-level output from A, B, C, or D through 3 levels of logic  |   |     | 17  | 30  | ns   |
| $t_{PLH}$ Propagation delay time, low-to-high-level output from A, B, C, and D through 2 levels of logic |   |     | 10  | 25  | ns   |
| $t_{PLH}$ Propagation delay time, low-to-high-level output from A, B, C, and D through 3 levels of logic |   |     | 17  | 30  | ns   |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



# SN5442A, SN54LS42, SN7442A, SN74LS42

## 4-LINE BCD TO 10-LINE DECIMAL DECODERS

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### recommended operating conditions

|                                       | SN54LS42 |     |      | SN74LS42 |     |      | UNIT         |
|---------------------------------------|----------|-----|------|----------|-----|------|--------------|
|                                       | MIN      | NOM | MAX  | MIN      | NOM | MAX  |              |
| Supply voltage, $V_{CC}$              | 4.5      | 5   | 5.5  | 4.75     | 5   | 5.25 | V            |
| High-level output current, $I_{OH}$   |          |     | -400 |          |     | -400 | $\mu$ A      |
| Low-level output current, $I_{OL}$    |          |     | 4    |          |     | 8    | mA           |
| Operating free-air temperature, $T_A$ | -55      |     | 125  | 0        |     | 70   | $^{\circ}$ C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                                    | TEST CONDITIONS†  | SN54LS42                |      |      | SN74LS42 |      |      | UNIT    |    |
|--|---|-------------------------|------|------|----------|------|------|---------|----|
|  |   | MIN                     | TYP‡ | MAX  | MIN      | TYP‡ | MAX  |         |    |
| $V_{IH}$ High-level input voltage            |   | 2                       |      |      | 2        |      |      | V       |    |
| $V_{IL}$ Low-level input voltage             |   |                         |      | 0.7  |          |      | 0.8  | V       |    |
| $V_{IK}$ Input clamp voltage                 | $V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$   |                         |      | -1.5 |          |      | -1.5 | V       |    |
| $V_{OH}$ High-level output voltage           | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$ | 2.5                     | 3.5  |      | 2.7      | 3.5  |      | V       |    |
| $V_{OL}$ Low-level output voltage            | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}$                            | $I_{OL} = 4 \text{ mA}$ |      | 0.25 | 0.4      | 0.25 | 0.4  | V       |    |
|  |   | $I_{OL} = 8 \text{ mA}$ |      |      |          | 0.35 | 0.5  |         |    |
| $I_I$ Input current at maximum input voltage | $V_{CC} = \text{MAX}, V_I = 7 \text{ V}$  |                         |      | 0.1  |          |      | 0.1  | mA      |    |
| $I_{IH}$ High-level input current            | $V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$  |                         |      | 20   |          |      | 20   | $\mu$ A |    |
| $I_{IL}$ Low-level input current             | $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$  |                         |      | -0.4 |          |      | -0.4 | mA      |    |
| $I_{OS}$ Short-circuit output current §      | $V_{CC} = \text{MAX}$   | -20                     |      | -100 |          |      | -20  | -100    | mA |
| $I_{CC}$ Supply current                      | $V_{CC} = \text{MAX}, \text{ See Note 2}$   |                         | 7    | 13   |          | 7    | 13   | mA      |    |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$ .

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2.  $I_{CC}$  is measured with all outputs open and inputs grounded.

### switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

| PARAMETER  | TEST CONDITIONS  | MIN | TYP | MAX | UNIT |
|--|--|-----|-----|-----|------|
| $t_{PHL}$ Propagation delay time, high-to-low-level output from A, B, C, or D through 2 levels of logic  | $C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega, \text{ See Note 3}$ |     | 15  | 25  | ns   |
| $t_{PHL}$ Propagation delay time, high-to-low-level output from A, B, C, or D through 3 levels of logic  |  |     | 20  | 30  | ns   |
| $t_{PLH}$ Propagation delay time, low-to-high-level output from A, B, C, and D through 2 levels of logic |  |     | 15  | 25  | ns   |
| $t_{PLH}$ Propagation delay time, low-to-high-level output from A, B, C, and D through 3 levels of logic |  |     | 20  | 30  | ns   |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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